



GE Fanuc Automation

Controller and I/O Products

VersaMax™ I/O and Control System Guide Form Specification

GFT-298

September 2002

1.1 SCOPE

1.1.1 *This specification covers the technical requirements for a control and/or I/O system. This system can function as a standalone programmable logic controller, distributed programmable logic controller, or as industrial I/O for a user-specified controller. The controller receives discrete and analog inputs and controls discrete and analog outputs in a manner dictated by the user-specified logic, which is written in controller languages called Relay Ladder Logic or Instruction List. The controller can also perform data handling operations and communicate with external devices.*

1.2 MANUFACTURER'S QUALIFICATIONS

1.2.1 MANUFACTURER'S STANDARDS

1.2.1.1 *The manufacturer shall have shown high commitment to product, manufacturing and design process quality. It shall have attained ISO9000 registration and utilise the Six Sigma quality standard in component manufacture.*

1.2.2 DESIGN AND MANUFACTURE

1.2.2.1 *The controller and/or I/O system and all of the corresponding components, shall be manufactured by GE-Fanuc Automation.*

1.2.2.2 *The manufacturer of the controller and/or I/O system must have a complete range of Automation products that include systems up to Safety Certification levels TUV6/ SIL3 and open-architecture VME control platforms that can accept third-party hardware.*

1.2.2.3 *The manufacturer's Automation products must include compatible, state-of-the-art SCADA/HMI software.*

1.2.2.4 *All products shall be designed, manufactured, and tested in accordance with recognized UL, CSA, IEC and JIS industrial standards. The system shall be operational during and after testing. See tables below for standards requirements.*

AGENCY APPROVALS OVERVIEW		<i>Comments</i>
Quality Assurance in Design/Development, Production, Installation & Servicing	ISO9001	Certification by Underwriters Laboratories and BSI Quality Assurance
Industrial Control Equipment [Safety]	UL508	Certification by Underwriters Laboratories
Process Control Equipment [Safety]	CSA22.2, 142-M1987 or C-UL	Certification by Canadian Standards Association or Underwriters Laboratories
	UL1604 with C-UL	Certification by Underwriters Laboratory
European EMC Directive	CE Mark	Certification by Competent Body for EMC Directive for selected modules

STANDARDS	<i>Conditions</i>
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OVERVIEW		
ENVIRONMENTAL		
Vibration	IEC68-2-6, JISC0911	1G @40-150Hz, 0.012in p-p @10-40Hz
Shock	IEC68-2-27, JISC0912	15G, 11ms
Operating Temperature		0°C to 60°C inlet
Storage Temperature		-40°C to +85°C
Humidity		5% to 95%, non-condensing
Enclosure Protection	IEC529	Steel cabinet per IP54: protection from dust & splashing water
EMC EMISSIONS		
Radiated, Conducted	CISPR11, EN55011 FCC	Class A [applies to CE Marked modules] part 15, subpart J, Class A
EMC IMMUNITY		
Electrostatic Discharge	IEC801-2	8KV Air Discharge, 4Kv Contact Discharge
Radiated RF	IEC801-3	10V _{rms} /m, 80Mhz to 1000Mhz, modulated
Fast Transient Burst	IEC801-4	2KV: power supplies, 1KV: I/O, communications
Surge Withstand	ANSI/IEEE C37.90a IEC255-4	Damped Oscillatory Wave, 2.5KV [cmn,diff mode]: power supplies, I/O [12V-240V] Damped Oscillatory Wave, Class II: power supplies, I/O [12V-240V]
Conducted RF	IEC801-6	10V, 150khz to 80Mhz injection for comm cables >30m
ISOLATION		
Dielectric Withstand	UL508, UL840, IEC664	1.5KV for modules rated from 51v to 250v
POWER SUPPLY		
Input Dips, Variations	IEC1000-4-11	During Operation: Dips to 30% and 100%, Variation for AC _10%, Variation for DC _20%
PROGRAMMING		
Software	IEC61131	Use of IEC address prefixes - %I for DI, %Q for DO, %M for Internal Bits, %AI for AI, %AQ for AO and %R for Internal 16 bit Registers

- 1.2.2.5 *The manufacturer shall have a fully operational quality assurance and quality control program in place conforming to the Six Sigma standard.*
- 1.2.2.6 *Complete documentation describing the quality assurance and quality plan shall be available.*
- 1.2.2.7 *Complete product documentation describing installation and simple field maintenance shall be available.*
- 1.2.3 **SUPPORT**
- 1.2.3.1 *Product shall have a warranty period of at least 1 year from the date of purchase.*

1.2.3.2 *The manufacturer or its authorized representative shall provide complete technical support for all of the products. This shall include headquarters or local training, regional application centers, and local or headquarters technical assistance. A toll-free number hot-line shall be available for emergency support.*

2 CRITICAL REQUIREMENTS

2.1 *It must be possible to program the controller and I/O through an integrated, custom object-oriented software environment that also allows creation of HMI applications, programming of electronic Operator Interface Touch-screens, and Windows NT and CE targets such as PCs etc. The software should include functions such as system management, a common database between control and HMI, and built-in web interfaces.*

2.2 *The same software package shall be used to program the manufacturer's entire range of controllers.*

2.3 *The controller shall be capable of being programmed by using a Flash memory device or card without the need of having a PC present. Programming the controller shall be initiated by pushing a button on the Flash device.*

2.4 *The hardware should allow for maximum versatility by being able to be used as either a stand-alone programmable logic controller, distributed programmable logic controller or as industrial I/O for a user-specified controller.*

2.5 *It should be possible to locate local I/O expansion units up to a distance of 750 metres from the CPU while using RS-485 differential communications.*

2.6 *Remote I/O units shall be auto-configuring. Configuration software or hand-held devices shall not be required to configure communication interfaces or remote I/O modules.*

2.7 *The network communications to be used must be deterministic Ethernet based, employing a "producer-consumer" protocol.*

3 GENERAL PRODUCT INFORMATION

3.1 *The system shall consist of rugged components designed specifically for industrial environments. A complete system shall consist of one or more stations containing DIN-rail-mounted I/O modules, I/O field wiring carriers, CPU or Network Interface Unit (NIU), and power supply interconnected by signal/power cables.*

3.2 PACKAGING

3.2.1 *All components shall be housed in structurally secure modules that are fully enclosed within a durable plastic shroud.*

3.2.2 *The system shall be modular and DIN rail mounted with added provisions for panel mounting. When mounted on the system base, each I/O module shall not occupy more than one available slot. The electronic components of each I/O module shall be separate from the I/O wiring carrier termination.*

3.2.3 *The depth of the system shall not exceed 70mm when mounted on a DIN rail with a power supply.*

- 3.2.4 *I/O modules shall be retained with a lock down mechanism.*
- 3.2.5 *The I/O modules shall have a color plastic insert for quick identification of the module as high voltage (red), low voltage (blue), signal level (gray), or mixed (gold) type.*
- 3.2.6 *I/O modules shall require no tools for insertion or extraction. Module insertion or removal shall not disturb field wiring.*
- 3.2.7 *Modules shall connect electrically via a pin and socket connector and be capable of insertion or removal without requiring disconnection of the mains supply.*
- 3.2.8 *All products shall be marked using a laser etching process that leaves all plastic housings recyclable. The markings shall be placed on the front of each product and include the manufacturer's catalog number, product manufacturing date code, and certifications.*

3.3 DURABILITY

- 3.3.1 *All components shall be manufactured with a high degree of durability.*
- 3.3.2 *All switches and other operator-controlled devices shall be of the size and durability for the intended use as is normally offered for industrial applications.*
- 3.3.3 *All signal cables furnished by the manufacturer shall be constructed so as to withstand, without damage, all normal use and handling.*

3.4 PARTS INTERCHANGEABILITY

- 3.4.1 *The I/O system shall have a keying system to prevent modules from being installed into the wrong field-wiring carrier.*
- 3.4.2 *Wherever possible, all assemblies and sub-assemblies performing similar functions shall be interchangeable.*

4 POWER SUPPLY

- 4.1 *The power supply shall be modular in design, separate from the CPU or Network Interface Unit, for easy replacement in the unlikely event of failure.*
- 4.2 *The power supply shall be compatible with main CPU or Network Interface Unit stations, as well as with expansion stations and booster power supply carriers.*
- 4.3 *The AC power supply shall operate at 85 to 132 VAC and 176 to 264 VAC at 27 VA of input power.*
- 4.4 *The DC power supply shall operate from an 18 VDC to 30 VDC voltage source requiring up to 11 Watts of input power (depending on module loading).*

5 CENTRAL PROCESSING UNIT (CPU)

- 5.1 *The CPU provided shall be modular. The CPU shall have the capability to solve application logic, store the application program, and store numerical values related to the application processes and logic, and interface to the I/O system. The CPU shall provide at least the following advanced*

- programming features: PID, Modulo, Math, Floating Point Math, Double Precision math, Logical functions, Subroutines, Data Array Move and Indirect Addressing.*
- 5.2 *The CPU shall contain a real-time calendar and clock that can be accessed by the user program. This Time of Day clock and calendar shall be battery-backed and maintain seven time functions: Year (4 digits), Month, Day of Month, Hour, Minute, Second, and Day of week and be year 2000 compliant.*
- 5.3 *The CPU shall execute Boolean instructions at a rate of 0.5 microseconds per instruction or faster.*
- 5.4 *The CPU shall be capable of controlling up to 8 local I/O carriers in the basic configuration and up to 56 additional I/O carriers remotely. The CPU shall support a total of 256 local I/O and a total of 4096 I/O in a local and remote configuration.*
- 5.5 *The CPU shall provide 2 serial ports, (1) 9 pin RS232 and (1) 15 pin RS485 for communications. Both ports shall support CPU programming. Both ports are configurable for SNP slave, Modbus RTU Master and slave operation and serial I/O data. Both ports shall support 4-wire and 2-wire Modbus[®] RTU. The CPU must also provide an integrated TCP/IP Ethernet port with a standard RJ-45 UTP connection. The Ethernet port shall support the Producer/Consumer method of communication.*
- 5.6 *Both serial ports on the CPU shall support configurable baud rates from 1.2kbps to 38.4 kbps.*
- 5.7 *The CPU shall support serial ASCII read and write for communication to non-standard serial devices.*
- 5.8 *Application programs, configurations, and data are maintained in non-volatile RAM and protected by a super-capacitor and/or optional battery. This data is saved if power is cycled to the CPU. Using the programmer, all data can be saved to flash memory, which does not require battery backup. The CPU can be configured to automatically restore data each time it powers up.*
- 5.9 *With a battery, data shall be retained for 3 months in storage or approximately 7 months with the CPU powered up for 50% of the time.*
- 5.10 *The battery shall be easily removed and readily available through commercial outlets.*
- 5.11 *There shall also be a super capacitor that provides a minimum of 1 to 2 hours battery-less backup power for CPU RAM memory.*
- 5.12 *The CPU shall provide LEDs, visible through the module's door, which indicate the presence of power and show the operating mode and diagnostic status of the CPU. The following LEDs shall be provided on the CPU:*
- *Power*
 - *OK*
 - *Run*
 - *Fault*
 - *Force*
 - *Port 1*
 - *Port 2*

5.13 ALARM PROCESSOR

- 5.13.1 *The CPU shall contain an alarm processor that is a special CPU feature designed to receive and process faults. The diagnostics shall provide information on the configuration and CPU, memory, communications and I/O status.*
- 5.13.2 *The alarm processor function shall log I/O and system faults in two fault tables that shall be accessible for display on the Windows® compatible programming software screen or uploaded to a host computer or other coprocessor.*
- 5.13.3 *The alarm processor shall maintain the states of up to 128 discrete system diagnostic bits to be read by a host or incorporated as contacts into the ladder program for customized diagnostic routines.*
- 5.13.4 *Each fault table shall have a total capacity of 32 faults. The last 16 entries shall maintain the latest 16 faults. The first 16 entries shall be kept unchanged.*
- 5.13.5 *Faults may be cleared by the user by way of a programmer. Provision shall be made by way of passwords to protect these faults from unauthorized clearing. Faults may also be cleared by a key switch.*

5.14 ALARM FEATURES

- 5.14.1 *The alarm processor shall report three types of fault action: fatal, diagnostic, or informational, and the CPU shall respond as follows:*

FAULT ACTION	FATAL	DIAGNOSTIC	INFORMATIONAL
<i>CPU Enters STOP Mode</i>	YES	NO	NO
<i>Set Diagnostic Bit</i>	YES	YES	NO
<i>Logged In Fault Table</i>	YES	YES	YES

- 5.14.2 *When an I/O fault occurs, the alarm processor shall report the station and slot location of the fault, the condition, the address and the circuit number if appropriate.*
- 5.14.3 *The alarm processor function shall have the capability to time-stamp system faults for future reference.*

5.15 SYSTEM SECURITY

5.15.1 CPU MEMORY PROTECTION

- 5.15.1.1 *The CPU shall have a minimum of 4 levels of security or password privilege levels to prevent unauthorized changes to the contents of the CPU. These built-in privilege levels shall be set in the programming software and shall impose the following constraints:*

Level	Constraint
1	<i>Read CPU data only (except passwords)</i>
2	<i>Write to any data memory</i>

3	#2 and write to all configuration or logic in STOP mode
4	#3 and write to logic in STOP or RUN mode (on-line change) and password level access

5.15.1.2 *There shall be one password, one to four ASCII characters in length, for each privilege level in the CPU, and the same password can be used for more than one level.*

5.15.1.3 *Any attempts to access or modify information in the CPU without the proper password privilege level shall be denied.*

5.15.2 SUBROUTINE PASSWORD

5.15.2.1 *The CPU shall have a software OEM key that allows users to control access to each subroutine in the relay ladder program.*

5.15.3 OEM PROGRAM PROTECTION

5.15.3.1 *The CPU shall have a software OEM key that allows users to protect the resident relay ladder program from unauthorized reads and writes.*

5.16 CPU MEMORY

5.16.1 MEMORY CAPACITY

5.16.1.1 *The CPU shall support at least the following resources:*

- *65,534 (64K), bytes for application programming memory*
- *16,384 (16K) 16-bit registers for register and data usage*
- *1280 global references*
- *2048 (2K) control relays*
- *2048 (2K) bits for discrete inputs*
- *2048 (2K) bits for discrete outputs*
- *256 16-bit registers for analog inputs*
- *256 16-bit registers for analog outputs*
- *256 bits discrete internal temporary*
- *1024 bit discrete internal with memory retention*

5.16.1.2 *Executive level operations performed by the CPU shall not consume application memory.*

5.16.2 MEMORY RETENTION AND DIAGNOSTICS

5.16.2.1 *The register values and the application program shall be stored in battery backed RAM. The application program and system configuration shall also be stored in non-volatile FLASH memory.*

- 5.16.2.2 *There shall be a long-life Lithium battery used to maintain the contents of the RAM in the CPU.*
- 5.16.2.3 *There shall be an easily accessible battery compartment in the CPU. The battery shall be replaceable with power applied to the CPU and without removing the CPU.*
- 5.16.2.4 *A low battery condition shall be alarmed with a system diagnostic bit.*
- 5.16.2.5 *The CPU shall update the application program checksum at the end of every sweep. A complete checksum calculation for a program may take multiple sweeps. A configurable number of program memory words shall be calculated each sweep. If the calculated checksum does not equal the reference checksum, a fault shall be recorded, and the CPU mode will change to STOP/FAULT.*

6 COMMUNICATIONS

6.1 CPU

6.1.1 CPU MASTER/SLAVE COMMUNICATIONS

- 6.1.1.1 *The CPU shall have the capability to communicate with external devices through Network Communications Modules supporting different networks.*
- 6.1.1.2 *One module shall allow the CPU to communicate as a slave on Profibus-DP.*
- 6.1.1.3 *One module shall allow the CPU to communicate as a master on DeviceNet™.*

6.2 DISTRIBUTED I/O COMMUNICATIONS

- 6.2.1 *When used as a distributed I/O system a networked master shall communicate with the I/O modules through a Network Interface Unit.*
- 6.2.2 *The following networks shall be supported as Network Interface Units:*
- *Genius®*
 - *Profibus-DP*
 - *DeviceNet*
 - *TCP/IP Ethernet*
- 6.2.3 *The Profibus-DP Network Interface Unit shall support a minimum of 125 nodes per bus.*
- 6.2.4 *The DeviceNet Network Interface Unit shall support a minimum of 63 nodes per bus.*
- 6.2.5 *The Genius Network Interface Unit shall support a minimum of 31 nodes per bus.*

7 I/O

7.1 FIELD WIRING INTERFACE

- 7.1.1 *The I/O modules shall be supported by individual field wiring carriers that connect the I/O electronics to the I/O bus. Each CPU and Network Interface Unit shall support eight I/O carriers locally and be expandable to 64 I/O carriers. The carriers shall be capable of accepting modules with up to 32 points.*
- 7.1.2 *There shall be at least four styles of I/O carrier wiring terminations – IEC box style, barrier style, spring clamp style, and connector style. The I/O carriers shall be universal and accept any discrete or analog I/O modules.*
- 7.1.3 *The I/O modules and carriers shall be the same for either direct connection to the CPU or connection to the Network Interface Unit as distributed I/O.*
- 7.1.4 *Each I/O carrier shall have a clear plastic door that covers the wiring terminals.*
- 7.1.5 *Each I/O carrier shall include a label with the module description, catalog number, and wiring diagram for that module type. The outside of the label shall have user legend space to record wiring information.*

7.2 I/O ADDRESSING

- 7.2.1 *I/O modules connected to a Network Interface Unit shall have reference addressing assigned automatically upon power up.*
- 7.2.2 *I/O reference addressing for modules connected to a CPU shall be assigned automatically upon power up or may be assigned through the use of the Windows compatible configuration and programming software.*
- 7.2.3 *There shall be no DIP switch settings required to address I/O modules.*

7.3 VISUAL DIAGNOSTICS

- 7.3.1 *Each I/O module shall have an OK LED to indicate when backplane power is present to the module.*
- 7.3.2 *Output modules shall have a field power LED to indicate when field power is applied to the module.*
- 7.3.3 *Each discrete I/O module shall have individual LEDs to indicate the on/off state of the I/O points.*
- 7.3.4 *The diagnostic status of the Electronic Short Circuit Protection (ESCP), for those discrete output modules containing ESCP, shall be indicated by a green LED during normal operation per point and amber during a fault. The fault should be auto-corrective without the need to cycle power.*

7.4 DISCRETE I/O

7.4.1 DISCRETE INPUT MODULE SPECIFICATIONS

- 7.4.1.1 *The 120 Volt AC input module shall accommodate an input voltage range of 85 to 132 volts. The 240 Volt AC input module shall accommodate an input voltage range of 155 to 264 volts.*
- 7.4.1.2 *The 24 Volt DC positive/negative logic input modules shall accommodate an input voltage range of 15 to +30 volts DC and nominal 24VDC.*

7.4.1.3 *The 48 Volt DC positive/negative logic input modules shall accommodate an input voltage range of 34 to +60 volts DC and nominal 48VDC.*

7.4.2 AVAILABILITY OF DISCRETE INPUT MODULES

7.4.2.1 *As a minimum, the following discrete input modules shall be available:*

Description	Points/Module
<i>120 VAC Input</i>	<i>8 and 16</i>
<i>240 VAC Input</i>	<i>8 and 16</i>
<i>48 VDC, Positive Logic Input</i>	<i>16 and 32</i>
<i>24 VDC, Positive Logic Input</i>	<i>16 and 32</i>

7.4.3 DISCRETE OUTPUT MODULE SPECIFICATIONS

7.4.3.1 *Grouped Discrete AC output modules shall have separate and independent commons allowing each group to be used on different phases of AC supply.*

7.4.3.2 *Each discrete AC output shall be provided with an RC snubber to protect against transient electrical noise on the power line.*

7.4.3.3 *Discrete AC outputs shall be suitable for controlling a wide range of inductive and incandescent loads by providing a high degree of inrush current (10x the maximum rated current).*

7.4.3.4 *Discrete DC output modules shall be available with positive logic characteristics in compliance with IEC industry standards.*

7.4.3.5 *Discrete DC output modules shall provide at least eight output points in a group with a common power input terminal per group. DC outputs shall also be available with Electronic Short Circuit Protection.*

7.4.3.6 *Discrete DC output modules shall be compatible with a wide range of user-supplied load devices, such as: motor starters, solenoids, and indicators.*

7.4.3.7 *A 2 Amp relay isolated output module shall be capable of supplying 2 Amps resistive maximum load per output.*

7.4.4 AVAILABILITY OF DISCRETE OUTPUT MODULES

7.4.4.1 *As a minimum, the following mixed I/O modules shall be available:*

Description	Points/Module
<i>120 VAC, 0.5A, Isolated</i>	<i>8 and 16</i>

Description	Points/Module
120 VAC, 2A, Isolated	8
24 VDC Positive Logic, 0.5A	16 and 32
24 VDC Positive Logic, 0.5A with Electronic Short Circuit Protection	16 and 32
24 VDC Positive Logic, 2A with Electronic Short Circuit Protection	8
Relay, Normally Open, 2A Isolated	8 and 16

7.4.5 AVAILABILITY OF DISCRETE MIXED I/O MODULES

7.4.5.1 As a minimum, the following mixed discrete I/O modules shall be available:

Description	Points/Module
24 VDC Input, Relay Output	20 Inputs and 12 Outputs 16 Inputs and 8
24 VDC Input, 24VDC Output with High Speed Counters and Pulse Width Modulation or Pulse Train Outputs	20 Inputs and 12 Outputs
24 VDC Input, 24VDC Output	16 Inputs and 16 Outputs
24 VDC Input, 24VDC Output with Electronic Short Circuit Protection	16 Inputs and 16 Outputs
120 VAC Input, 120 VAC Output	8 Inputs and 8 Outputs
120 VAC Input, Relay Output	8 Inputs and 8 Outputs
240 VAC Input, Relay Output	8 Inputs and 8 Outputs

7.5 ANALOG I/O

7.5.1 ANALOG INPUT VOLTAGE /CURRENT MODULES

7.5.1.1 The analog voltage/current input modules shall be capable of converting a minimum of 4 channels of inputs in the range of -10 to +10 volts, 0 – 10 volts, and 4mA to 20mA.

7.5.1.2 Resolution of the converted analog voltage/current input signal shall be available in 12 bit and 16 bit versions.

7.5.1.3 All of the channels of converted analog voltage/current input signals shall be updated each scan into a dedicated area of data registers in a 16-bit 2's complement format.

7.5.1.4 The conversion speed for all of the analog voltage/current input channels shall be no less than 2 milliseconds and no greater than 13 milliseconds.

7.5.2 ANALOG OUTPUT VOLTAGE MODULES

- 7.5.2.1 *One analog voltage output module shall be capable of converting 4 channels of digital data to analog outputs in the range of -10 to +10 volts.*
- 7.5.2.2 *One analog voltage output module shall be capable of converting 4 channels of digital data to analog outputs in the range of 0 to +10 volts.*
- 7.5.2.3 *Resolution of the converted output signal shall be 12 bits.*
- 7.5.2.4 *All channels of analog output data shall be updated each scan from a dedicated area of data registers in a 16-bit 2's complement format.*
- 7.5.2.5 *The analog voltage outputs default to hold-last-state in the event of a CPU failure according to the following table:*

Module	Default	Configurable power loss state
0-10 V	Hold last state	0 V
-10 V to +10 V	Hold last state	0 V

7.5.3 ANALOG OUTPUT CURRENT MODULES

- 7.5.3.1 *An analog current output module shall be capable of converting 4 channels of digital data to analog outputs in the range of 4 to 20 mA. .*
- 7.5.3.2 *Resolution of the converted output signal shall be 12 bits.*
- 7.5.3.3 *All channels of analog output data shall be updated each scan from a dedicated area of data registers in a 16-bit 2's complement format.*
- 7.5.3.4 *The analog current outputs shall be configurable to default to 0 current or hold-last-state in the event of a CPU failure.*

7.5.4 ANALOG MIXED MODULES

- 7.5.4.1 *Analog mixed modules shall be capable of converting 4 channels of analog inputs to digital data and 2 channels of digital data to analog outputs.*
- 7.5.4.2 *There shall be one analog mixed module that supports 4 channels of 4 to 20 mA inputs and 2 channels of 4 to 20 mA outputs. Another module shall be available that supports 4 channels of 0 to 10 VDC inputs and 2 channels of 0 to 10 VDC outputs.*
- 7.5.4.3 *All channels of analog data shall be updated each scan from a dedicated area of data registers in a 16-bit 2's complement format.*
- 7.5.4.4 *The analog outputs shall be configurable to default to 0 volts/4 mA or hold-last-state in the event of a CPU or network failure.*

7.5.5 ANALOG I/O MODULE AVAILABILITY

7.5.5.1 As a minimum, the following analog modules shall be available:

Description	Channels/Module
Analog Input Voltage/Current	4, 8 and 15
Analog Input RTD	4
Analog Input Thermocouple	7
Analog Output Current	4
Analog Output Voltage	4, 8 and 12
Analog Inputs/Outputs Current	4 Inputs and 2 Outputs
Analog Inputs/Outputs Voltage	4 Inputs and 2 Outputs

7.6 SPECIALTY MODULES

7.6.1 HIGH SPEED COUNTER/PWM/PT MODULE

7.6.1.1 A specialized high speed counter/PWM/PT option module shall be available to accommodate applications where pulse input rates exceed the input capability of the CPU or where high speed pulsed outputs are required.

7.6.1.2 The high speed counter module shall have 20 DC Inputs and 12 DC outputs. Up to 4 of the 20 inputs shall be configureable as high speed counter inputs. The other inputs are available for use as discrete inputs. Up to 4 of the 12 discrete outputs may be configured as Pulse Width Modulated outputs or Pulse Train outputs.

7.6.1.3 The module may be configured as a high speed counter or high speed output module.

7.6.1.4 As a high speed counter, the module shall be configurable as four independent counters counting either up or down (uni-directional), one independent bi-directional counter and two uni-directional counters, or one bi-directional counter that can perform a homing sequence.

7.6.1.5 As a high speed output module the module shall produce up to four PWM or PT outputs up to 5 KHz.

8 PROGRAMMING

8.1 GENERAL

- 8.1.1 *A Software programming package running on a PC compatible laptop or desktop computer shall be used to program the CPU. The software shall be Windows 98, Windows 2000, Windows XP and Windows NT[®] compatible.*
- 8.1.2 *On-line and off-line, CPU and I/O configuration and application program development shall be achieved with the PC compatible computer and programming and documentation software.*
- 8.1.3 *The PC compatible computer shall be connectable to the CPU via a built-in serial communication port or TCP/IP Ethernet port on the CPU.*
- 8.1.4 *The software shall be capable of programming a Flash memory device or card for later storage to the controller.*
- 8.1.5 *The programming software shall have access to the application program, the CPU and I/O system configurations, all registers, CPU and I/O status, system diagnostic relays, and I/O over-ride capabilities*

8.2 WINDOWS COMPATIBLE SOFTWARE

- 8.2.1 *The Windows compatible software shall provide the capability of reading, writing, and verifying the configuration and program with a diskette backup.*
- 8.2.2 *The software shall execute on a Windows 98, Windows 2000, Windows XP and Windows NT[®] platform.*
- 8.2.3 *The software shall provide on-screen help information throughout its execution paths.*
- 8.2.4 *The software shall have the capability of programming the user logic, store the program to the CPU, monitor program and reference address status while the CPU is in Run or Stop mode.*
- 8.2.5 *The software shall support complete Windows functionality, including:*
 - *Drag and drop within the application*
 - *Drag and drop to external applications, such as Microsoft[®] Excel and Word.*
- 8.2.6 *The programming software shall support bumpless run mode storage of the program to the CPU.*
- 8.2.7 *The software shall be capable of programming the manufacturer's entire range of controllers.*
- 8.2.8 *The software shall be capable of generating a printout of the relay ladder program for documentation purposes. The user shall be able to select any of the program documentation below:*

Types of Documentation	Description
<i>Print Program</i>	<i>This printout shall print the program logic with or without the equivalent Boolean instructions for each rung, the reference list, reference descriptions and/or users rung comments.</i>
<i>Cross reference tables</i>	<i>This printout shall show the use of references in the program.</i>
<i>Reference tables</i>	<i>This printout shall show the values of each reference in each selected table.</i>
<i>Configuration Printout</i>	<i>This printout shall allow the user to generate a rack hardware and its assigned reference address listing, and the CPU configuration listing.</i>

- 8.2.9 *The software shall support the creation of an electronic representation of the logic, as a bit map, to display in other documentation tools.*
- 8.2.10 *The software shall provide the capability for programming using user-defined variables (nicknames).*
- 8.2.11 *The software shall have built-in modem connection capabilities.*
- 8.2.12 *The software shall be IEC 61131 compliant and support the use of standard IEC address prefixes where %I represents digital inputs, %Q represents digital outputs, %M represents internal bits, %AI represents analog inputs, %AQ represents analog outputs and %R represents internal 16 bit registers.*
- 8.2.13 *The software shall have provisions for importing and exporting tag names, comments and descriptions in an .xls format.*
- 8.2.14 *The software shall support toggle/override capability and mixed reference tables for viewing I/O status.*
- 8.2.15 *The software shall be capable of displaying controller digital and analog data in a trend display screen.*
- 8.2.16 *The software shall provide data watch windows that permit drag and drop of variables and logic directly into the window.*
- 8.2.17 *The software shall support the use of classes and objects for user logic.*
- 8.3 PROGRAMMING LANGUAGES**
- 8.3.1 *The CPU shall be capable of solving an application program whose source format shall be relay ladder diagram (LD) or Instruction List (IL).*
- 8.3.2 RELAY LADDER DIAGRAM FUNCTIONS**
- 8.3.2.1 *Relay ladder operations shall consist of the following contacts and coils:*
Relay Functions
Normally Open Contact
Normally Closed Contact
Coil
Negated Coil
Retentive Coil
Negated Retentive Coil
Positive Transition Coil
Negative Transition Coil
Set Coil (Latch)
Reset Coil (Unlatch)
Retentive Set Coil
Retentive Reset Coil
- 8.3.2.2 *Positive transition coils and negative transition coils shall function as leading and trailing edge one-shot coils respectively.*
- 8.3.2.3 *Contacts may be referenced any number of times within the application program.*

- 8.3.2.4 *A single rung may contain more than one coil.*
- 8.3.2.5 *There shall be a service that allows user programs to be checked for multiple coil use. This flag may be set to:*
- *Disallow more than one coil in a single rung*
 - *Allow multiple coil use but generate warning messages*
 - *Allow multiple coil use without warnings*

8.3.3 TIMERS AND COUNTERS

- 8.3.3.1 *Timer and counter operations shall consist of the following types:*

Timer and Counter Functions

Retentive On-Delay Timer (ONDTR)

Simple Off- Delay Timer (OFDT)

Simple On-Delay Timer (TMR)

Up Counter (UPCTR)

Down Counter (DNCTR)

- 8.3.3.2 *The retentive on-delay timer shall behave as a stopwatch that increments time when enabled and holds the current timed value until receiving power flow to the reset input.*
- 8.3.3.3 *The simple on-delay timer shall increment while it receives power flow and reset to zero when power flow stops.*
- 8.3.3.4 *The simple off-delay timer shall increment while it power flow stops and reset to zero when power flow is present.*
- 8.3.3.5 *There shall be at least 682 programmed timers and/or counters available for use in application programs.*
- 8.3.3.6 *Each timer or counter requires the use of three 16-bit registers within %R register memory for storage of the preset, the current value and a control word. These three registers shall be accessible to the user via a register reference.*
- 8.3.3.7 *The timers and counters shall not require an output reference, the output of a timer or counter can be used to energize a coil, or enable another function, such as a math function, or another timer or counter.*
- 8.3.3.8 *The time/count limit shall be either a programmed constant or shall be programmable via a register reference value.*
- 8.3.3.9 *The time shall be counted in tenths of seconds, hundredths of seconds or thousandths of seconds, and the range for the timers and counters is 0 to 32,767 time units.*

8.3.4 ARITHMETIC

- 8.3.5 *The arithmetic operations shall support three data types, Floating Point (Real), Signed Integer (INT), and Double Precision Integer (DINT). Arithmetic functions shall consist of the following types:*

Arithmetic Functions

Addition

Subtraction

Multiplication

Division (quotient)

Modulo (remainder)

Square Root

Radian Conversion

Logarithmic and Exponential Functions

Trigonometric Functions

- 8.3.5.1 *Signed Integers (INT) data shall be stored in 16 contiguous bits of memory, in 2's complement notation. The range for Signed Integer Data shall be -32,768 to +32,767.*
- 8.3.5.2 *Double Precision Integer (DINT) data shall be stored in 32 contiguous bits of memory; double precision data is always signed. The range for Double Precision Integer Data shall be -2,147,483,648 to 2,147,483,647.*
- 8.3.5.3 *Floating Point (Real) data shall be stored in 32 contiguous bits of memory. This data is always signed. The range for Floating Point Data shall be $\pm 1.401298E-45$ to $\pm 3.402823E+38$*
- 8.3.5.4 *The arithmetic function blocks shall consist of 3 inputs and 2 outputs. The enable input shall begin the execution. When the function is enabled, the two data inputs are operated upon and the result is output. There shall also be an OK output that is always true when the function is enabled, unless an overflow or other error exists.*
- 8.3.5.5 *All of the Arithmetic functions shall be such that they can be cascaded together in a single rung.*

8.3.6 RELATIONAL FUNCTIONS

- 8.3.6.1 *Relation Functions which are used to compare two numbers, shall operate on Floating Point, Signed Integer and Double Precision Integer data types, and shall consist of the following types:*

Relational Functions

Equal To, Not Equal To

Greater Than, Greater Than or Equal to

Less Than, Less Than or Equal to

Range

8.3.6.2 *A method of checking for a value to be contained within a group of values shall be provided in a Range function.*

8.3.7 BIT OPERATION FUNCTIONS

8.3.7.1 *Bit Operation Functions shall perform comparison and movement operations on word data that is specified as a continuous string of data in 16-bit increments. The first bit of the first word being the least significant bit, and the last bit of the last word being the most significant bit.*

8.3.7.2 *Bit Operation Functions that are used to perform Boolean operations on corresponding bits of two bit strings of the same length shall consist of the following types:*

Boolean Functions

Logical AND

Logical OR

Logical Exclusive OR

8.3.7.3 *Bit Operation Functions used to create an output string that is a copy of an input bit string, but with its bits inverted, shifted, or rotated shall consist of the following types:*

Bit Functions

Logical Invert (NOT)

Shift Left

Shift Right

Rotate Left

Rotate Right

8.3.7.4 *The shift functions shall allow for the user to specify the number of places that the array is to be shifted as an input, and provide the state of the last bit shifted out, and a copy of the shift register as outputs.*

8.3.8 DATA MOVE FUNCTIONS

8.3.8.1 *Basic data movement capabilities shall be provided by the following list of functions:*

Data Move Functions

Move

Block Move

Block Clear

Shift Register

Bit Sequencer

Communications Request

- 8.3.8.2 *The movement of data (16 bit integer or word), as individual bits, from one location to another shall be accomplished by the Move function. The user shall be able to specify the length of the move.*
- 8.3.8.3 *The Block Move function shall provide the functionality to move a block of 7 constants (integer or word) to a specified location.*
- 8.3.8.4 *The ability to fill a specified block of data (word) with zeros shall be accomplished by the Block Clear function. The user shall be able to specify the length of the block.*
- 8.3.8.5 *The Shift Register function shall provide the functionality to shift one or more data words from a reference location into a specified memory location. All of the data within the Shift Register shall be accessible throughout the program from logic addressed memory.*
- 8.3.8.6 *A method of shifting a bit sequence through an array of bits shall be provided by a Bit Sequencer function. The function shall provide the ability to reset the sequence, change the direction of the bit pattern, or access the step location within the array.*
- 8.3.8.7 *Provisions to initiate communications with a specialized communication module shall be made through the use of a Communication Request function. This function shall allow the CPU to behave as a master on a serial communication link, thus providing the ability to communicate master/slave or peer to peer with any controller or computer using the same serial communication protocol.*
- 8.3.9 **TABLE FUNCTIONS**
- 8.3.9.1 *Table operations shall consist of moving data into or out of tables and searching for data of values equal to, not equal to, greater than, greater than or equal to, less than and less than or equal to a specified value.*
- Table Functions
Array moves
Search Equal
Search Not Equal
Search Greater Than
Search Greater Than or Equal to
Search Less Than
Search Less Than or Equal to
- 8.3.9.2 *The array move feature shall be capable of implementing indirect addressing applications.*
- 8.3.10 **CONVERSION FUNCTIONS**

8.3.10.1 *Conversion functions shall be provided to convert a data item to or from 4 digit Binary Coded Decimal (BCD-4) data type, 16 bit signed integer, 32 bit signed integer and 32 bit floating point data types.*

8.3.11 CONTROL FUNCTIONS

8.3.11.1 *Control functions shall be provided to limit program execution, alter the way the CPU executes the application program, or provide special CPU services. The following Control Functions shall be provided:*

Control Functions

CALL subroutine

Immediate I/O update (DO I/O)

Comment rung

Master Control Relay (MCR, END MCR)

Jump to a label (JUMP, LABEL)

Special Service Requests (SVCREQ)

Drum sequencer

8.3.11.2 *An immediate I/O update function shall be provided for the update of all or a portion of the inputs or outputs for one scan while the program is running, or to update I/O during the program in addition to the normal I/O scan.*

8.3.11.3 *Additionally, the function shall provide a means to read inputs into memory auxiliary to the true input table, and execute outputs from discrete memory alternate to the true output table.*

8.3.11.4 *A comment rung function shall be provided to enter a rung explanation in the program. The rung explanation shall have the capacity to hold 2048 characters of text. The memory required for the comment shall be independent of the program storage memory. The comment shall have the ability to be edited via the PC compatible programming software.*

8.3.11.5 *A master control relay function shall allow all rungs between the MCR and its subsequent END MCR function to be executed without power flow.*

8.3.11.6 *A method for structuring the ladder program shall be provided with the use of a JUMP Function. This will cause the program execution to jump to a specified location in the logic targeted by the location of the LABEL function.*

8.3.11.7 *Seven different special CPU service requests shall be accessible by the programmer by utilizing one of the Service Request Functions listed below:*

Service Request Functions

Change/Read Checksum Task State and

Logical Number of Words to Checksum

Change/Read Time of Day Clock.

*Shut Down the CPU.
Clear Fault Tables.
Read Last Fault Table Entry.
Read Elapsed time Clock.
Read I/O Override Status.*

8.3.11.8 *The Data written by these service request functions shall be in BCD or Packed ASCII format, and written into user definable register locations.*

8.3.12 *PID FUNCTION*

8.3.12.1 *A single PID function block instruction must be provided by the CPU without requiring any additional module. Two versions of this closed loop control algorithm (Proportional/Integral/Derivative) shall be available:*

8.3.12.2 *The standard ISA PID algorithm, which applies the proportional gain to each of the proportional, derivative, and integral terms; and*

8.3.12.3 *The independent algorithm that applies the proportional gain only to the proportional gain term.*

8.3.12.4 *The PID function block shall permit manual operation and include an integrated loop tuning and data display screen which shall allow tuning of the following loop parameters :*

PID Loop Parameters
P, I and D terms
Sample Period
Bias
Upper and Lower Deadbands
Upper and Lower Clamps
Error Term
Slew Rate
Derivative Action
Output Polarity

8.3.13 *SUBROUTINE FUNCTION*

8.3.13.1 *A single function block must be available to allow repetitive call of a function. A password to protect the integrity of the subroutine must also be available.*

8.3.13.2 *A Subroutine may be called from within another subroutine. The nesting must be at least 8 deep.*

8.3.13.3 *A Periodic Subroutine shall be available that is executed once a programmable interval elapses. The interval shall be between 1 and 10 milliseconds. The*

accuracy of the subroutine execution shall be 50 nanoseconds. Discrete I/O shall be available to update during the execution of the subroutine.

8.3.13.4 *The user may create up to 64 subroutines. The subroutine must allow a minimum of 16K bytes of user logic*

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